SEMESTER I

21LV01 GRAPH THEORY AND OPTIMIZATION TECHNIQUES

3 1 0 4

GRAPH THEORY: Common families of graphs, degree sequence, handshaking lemma, Havel-Hakimi theorem (statement only). Walk, trail and path, connected graph, distance, radius and diameter. Graph isomorphism. Representations of graphs – adjacency and incidence lists - adjacency and incidence matrices. (11+4)

GRAPH ALGORITHMS: Trees, spanning trees. Search algorithms – depth first search and breadth first search, spanning tree algorithm–Kruskal's and Prim's, shortest path algorithm–Dijkstra's flow networks: flows and cuts in networks, solution of the maximum - flow problem – characterization of maximum flow - Max-flow Min-cut Theorem (statement only), algorithms – maximum flow, augmenting path, and FFEK – maximum flow. (12+4)

LINEAR PROGRAMMING: Formulation, simplex method, two phase method, simplex multipliers, dual and primal. Transportation model – initial basic feasible solution- north-west corner rule, least-cost method, Vogel's approximation method, and optimum solution of transportation problem**.** (11+4)

DYNAMIC PROGRAMMING: Principle of optimality, backward and forward recursion, calculus method of solution, tabular method of solution, shortest-route problem, Knapsack model. (11+3)

Total L: 45 +T:15 = 60

REFERENCES:

1. Douglas B West, "Introduction to graph Theory", Pearson Education, New Delhi, 2018.
2. Hamdy A Taha, "Operations Research: An Introduction", Pearson Education, New Delhi, 2017.
3. Jonathan L Gross and Jay Yellen, "Graph Theory and its Applications", Chapman & Hall, New York, 2006.
4. Kambo N.Singh., "Mathematical Programming Techniques", East – West Press, New Delhi, 2012.
5. NarasinghDeo, "Graph Theory: with applications to engineering and computer science", PHI Learning, 2017.

21LV02 DESIGNING WITH FPGAS

2 2 0 4

VERILOG: Signals, Identifier, Net and variable types, Operators, Gate instantiations, Modules and ports, data flow, gate level, Behavioral level ,Switch level and state machine modeling , Concurrent and procedural statements, UDP, sub circuit parameters, function and task, timing and delays - test benches-design of combinational and sequential circuits using Verilog. (10+10)

FPGA ARCHITECTURES: Design flow using FPGAs, Role and Types of CAD Tools - Architecture of Xilinx and Altera FPGAs –configurable logic blocks, I/O blocks - programmable interconnections - Partial Reconfiguration on FPGAs- clock circuits – programming technologies – antifuse, SRAM, EPROM, EEPROM - Implementation using FPGA – Static Timing Analysis - timing models – critical path - calculation of maximum clock frequency - power analysis. (6+6)

CONTROL PATH AND DATA PATH DESIGN: Design of memories - ROM, single and dual port RAM - synchronous and asynchronous read - arithmetic circuit design - serial/parallel adder, subtractor, floating point adder/subtractor multiplier - sequential multiplier, array multiplier, signed multiplier – ALU – Hardwired Control Design – Micro programmed Control Design. (8+8)

CONTROLLER AND DSP DESIGN: Memory controller, processor control unit, communication controllers - UART, I^2C, VGA controller, USB, DSP blocks- FIR and IIR filters. (6+6)

Total L: 30 + T:30 = 60

REFERENCES:

1. Morris Mano M, Charles R Kime, "Logic and Computer Design Fundamentals", Pearson Education, 2015.
2. Charles H. Roth, "Digital system design using VHDL", Thomson, 2014.
3. Seetharaman Ramachandran, "Digital VLSI systems design", Springer, 2011.
4. Michael D Ciletti, "Advanced Digital Design with Verilog HDL", Pearson education, 2005.
5. Samir Palnitkar, "Verilog HDL: A Guide to Digital Design and Synthesis", Prentice Hall, 2003.

21LV03 DEVICE MODELLING

3 0 0 3

INTRODUCTION TO SEMICONDUCTOR PHYSICS AND DIODE MODELLING: Review of Quantum Mechanics - Boltzman transport equation - Continuity equation - Poisson equation. Junction and Schottky diodes in monolithic technologies - static and dynamic behavior - small and large signal models - SPICE models. (12)

INTEGRATED MOS CAPACITANCE : :Band diagram- flatband condition and flat band voltage-surface accumulation, surface depletion-thershold condition and threshold voltage, charge versus gatevoltage, MOS C-V Characteristics, Poly Si gate depletion-effective Increase In Tox. (8)

VLSI FABRICATION TECHNIQUES: An overview of wafer fabrication, wafer processing- oxidation - patterning - Diffusion - Ion implantation - Deposition - Silicon Gate nmos process - CMOS process - nwell - pwell -Twin tub - Silicon on Insulator - CMOS process enhancements - Interconnects circuit elements. (10)

INTEGRATED MOS TRANSISTOR: NMOS and PMOS Transistor - Threshold voltage - Threshold voltage equations - MOS device equations - Basic DC equations Second order effects - Small signal AC Characteristics- MOS models SPICE model, EKV Model, BSIM Model. Technology scaling for cost, speed and power consumption, Subthreshold Current –Subthreshold Swing, Threshold voltage Roll Off-Short Channel Leakage, reducing gate insulator electrical thickness And Tunneling Leakage, Short Channel Effects. Ultra Thin body, SOI and Multigate MOSFET - FINFET. MOSFET Compact Model for Circuit Simulation using Verilog-A. (15)

Total L: 45

REFERENCES

1. Tyagi M S, "Introduction to Semi-conductor Materials and Devices", John Wiley, 2008.
2. Chenming C.Hu, ”Modern Semiconductors for Integrated Circuits”, Prentice Hall, 2010.
3. Richard S. Muller,Theodore I. Kamins, Mansun Chan, "Device electronics for integrated circuits”, John Wiley, 2003.
4. Yannis Tsividis, ”Operation and modeling of the MOS transistor” Oxford University Press, 2010.
5. Neil Weste and David Harris, "A Circuits and Systems Perspective”, Pearson, 2010.

21LV04 DIGITAL IC DESIGN

3 0 0 3

OVERVIEW OF VLSI DESIGN METHODOLOGY: VLSI design process - Architectural design - Logical design-Physical design-Layout styles - Full custom, Semicustom approaches, layout design rules**:** Need for design rules – Layer representations - CMOS nwell / pwell design rules – Design rule backgrounder-Layer assignments-SOI rules. (11)

MOS INVERTER: Static characteristics-Resistive load inverter - Inverter with n-type MOSFET load - CMOS inverter - Transient characteristics-Delay time definitions, calculation of delay times. (11)

LOGIC DESIGN: Static CMOS Design-Complementary CMOS, Ratioed logic,Pass transistor and transmission gate - Dynamic CMOS logic - CMOS logic - Precharged domino logic- Static Sequential circuits-Bistatbility, CMOS static FF, Dynamic sequential circuits – Pseudo static latch, Dynamic two phase FF, Clocked- CMOS latch, NORA CMOS logic, TSPCL logic. (11)

VLSI BUILDING BLOCKS DESIGN: Adders, Shifters, Arithmetic logic unit design, Multipliers-Array, Carry Save, Wallace tree, Booth's algorithm, Modified Booth's Algorithm. Designing Memory and Array Structures-Memory peripheral circuit. (12)

Total L: 45

REFERENCES:

1. Jan M Rabaey, “Digital Integrated Circuits", Prentice Hall, second edition, 2016.
2. Kang, “CMOS Digital integrated Circuits”, McGraw Hill, 2016.
3. Neil Weste and David Harris, “CMOS VLSI Design: A Circuits and Systems Perspective”, Pearson, 4th edition 2015.
4. Douglas A Pucknell, Kamran Eshraghian, "Basic VLSI Design", PHI learning, New Delhi, 2011.
5. Saida M Sait and Habib Youssef, “VLSI Physical Design Automation: Theory and Practice”, World Scientific Publishing Company, 1999.

21LV05 VLSI TESTING

3 1 0 4

FAULT SIMULATION AND COMBINATIONAL CIRCUIT TESTING: Need for testing and design for testability - Fault models - Fault simulation techniques-Serial, Deductive, Parallel and Concurrent Simulation. Test generation algorithms for combinational logic circuits - Fault Table, Boolean difference, Path sensitization, D - algorithm PODEM, FAN algorithms. Path and delay fault testing (15+4)

SEQUENTIAL CIRCUIT TESTING AND DESIGN FOR TESTABILITY: Functional testing –Fault model based testing- Time frame expansion, Key testability concepts – Ad Hoc design for Testability – scan based design - Signature analysis - Compression techniques (10+4)

BIST AND MEMORY TESTING : Built-in self-test -Architectures-Boundary scan standard- Boundary scan architectures for Board level testing- FPGA testing. Memory: Fault models- Test algorithms-BIST architectures for memory –Testable memory design – Test generation for embedded RAM (12+4)

FAULT DIAGNOSIS : Logical Level Diagnosis – Diagnosis by UUT reduction – Fault Diagnosis for Combinational Circuits– Self-checking design – System Level Diagnosis. (8+3)

Total L: 45+ T:15 = 60

REFERENCES:

1. Wang, Wu and Wen, "VLSI Test Principles and Architectures", Morgan Kaufmann, 2006.
2. Vishwani D Agarwal, "Essential of Electronic Testing for Digital, Memory and Mixed Signal Circuits", Springer, 2005.
3. N.K.Jha, S.Gupta, "Testing of Digital systems", Cambridge university press, 2003.
4. Parag K Lala, "Digital Circuit Testing and Testability", Academic Press, 1997.
5. Abramovici M, Breuer M A and Friedman A D, "Digital Systems Testing and Testable Design", Wiley, 1994

21LV06 Research Methodology and IPR

vide Automotive Engineering 21AE06

21LV72 AUDIT COURSE I

vide Automotive Engineering 21AE72

21LV51 SCRIPTING AND SYSTEMVERILOG LABORATORY

0 0 4 2

- Basic constructs of Scripting Languages
- Report Analysis
- EDA Tool Automation
- Basic constructs of SystemVerilog
- SystemVerilog for verification
- OOPS concepts in SystemVerilog

Total P: 60

21LV52 MICROELECTRONICS SIMULATION LABORATORY

0 0 4 2

- Modeling of PN junction and Schottky diodes and plotting device characteristics
- Modeling of PMOS and NMOS devices and plotting transfer and output characteristics.
- Modeling of SOI, multigate, UTB and FINFET devices plotting transfer and output characteristics
- Spice model, EKV Model and BSIM model parameter extractions
- Verifying Model parameters with extracted parameters for CMOS inverter
- Study of MOS capacitor and Inverter characteristics
- Design of static and dynamic digital circuits
- Design of Memories with Peripherals

Total P: 60

SEMESTER II

21LV07 ANALOG VLSI CIRCUITS

3 1 0 4

ANALOG CIRCUIT BUILDING BLOCKS: Switches, Active resistors, Current sources and sinks, Current mirrors, Voltage references, Comparator, Multiplier, Single source amplifiers – Common source, Common drain and common gate. (11+4)

AMPLIFIERS: MOS inverting amplifier - Improving performance of inverting amplifier - CMOS differential amplifiers – Qualitative and Quantitative Analysis, Characterization of Op-Amp - CMOS two stage op-amp -Op-amps with output stage, Folded Cascode op-amp, Transconductance Amplifier-Noise and Distortion in Amplifiers. (12+4)

PHASE LOCKED LOOPS: Phase Detector-Voltage Controlled Oscillator-Loop Filter. Non-linear analog blocks: Comparators, Charge-pump circuits, and Multipliers, Analog Testing methods. LAYOUT ISSUES: Capacitors – Resistors - Mixed layout issues: Floor planning, power supply & ground, fully differential matching, Guard rings and shielding. (11+3)

DATA CONVERTER FUNDAMENTALS: Ideal A/D and D/A converters, Quantization noise, Signed codes, Performance limitations. D/A AND A/D CONVERTERS: D/A converter : Current scaling, Voltage scaling and Charge scaling D/A converters - Serial D/A converters -Serial A/D converters, Parallel - A/D converters. (11+4)

Total L: 45 + T: 15 = 60

REFERENCES:

1. Phillip Allen and Douglas Holberg, “CMOS Analog Circuit Design”, Oxford University Press, 2012.
2. Jacob Baker, “CMOS, Circuit Design Layout and Simulation”, Wiley- IEEE Press, 2011.
3. Randall L Geiger, Phillip E Allen and Noel R Strader, "VLSI Design Techniques for Analog and Digital Circuits", McGraw Hill, International Edition, 2010.
4. David A Johns and Ken Martin, “Analog Integrated Circuit Design”, John Wiley and Sons, 2008.
5. Benhard Razavi, “Data Converters”, Kluwer Publishers, 2005.

21LV08 HARDWARE VERIFICATION TECHNIQUES

3 0 0 3

VERIFICATION TECHNOLOGIES AND TOOLS: Importance of Verification - Reconvergence Model - The Human Factor - Formal and Functional Verification Approaches - Formal Verification - Boolean Functions, Approaches Based on Finite State Machines, Propositional Temporal Logics - Timing Verification - Testing Versus Verification - Design and Verification Reuse - Linting - Simulation - Third Party Models - Verification Intellectual Property - Waveform Viewers - Issue Tracking – Metrics - Role of the Verification Plan - Levels of Verification - Verification strategies - High-level modeling. (12)

SYSTEMVERILOG ASSERTIONS AND FUNCTIONAL COVERAGE: Immediate Assertions - Concurrent Assertions - Sampled Value Functions - System Functions and Tasks - Asynchronous Assertions - Multiple Clocks - Functional Coverage - Gathering Coverage Data - Coverage Types - Functional Coverage Strategies - Anatomy and Triggering of a Cover Group - Data Sampling - Cross Coverage - Generic Cover Groups - Coverage Options - Analyzing Coverage Data - Performance Implications of Coverage Methodology. (10)

TEST CASE GENERATION AND ARCHITECTING TESTBENCHES: Simple Stimulus - Simple Output - Complex Stimulus - Bus-Functional Models - Response Monitors - Transaction Level Interface - Verification Harness - Design Configuration - Self-Checking Test benches - Directed Stimulus - Random Stimulus - System Level Verification Harnesses - Transaction Level Models - Managing Simulations - Regression. (12)

VERIFICATION METHODOLOGY: Universal Verification Methodology (UVM) – Packages – Components – Environmental Structure – Factory Registration – Reporting. (11)

Total L: 45

REFERENCES:

1. Janick Bergeron, “Writing Test Benches Using System Verilog”, Springer 1st Edition, 2009.
2. Chris Spear, Greg Tumbush, "System Verilog for Verification - A Guide to Learning the Test bench Language Features" Springer 3rd edition, 2012.
3. Ashok B. Mehta, "SystemVerilog Assertions and Functional Coverage Guide to Language, Methodology and Applications", Springer, 2014.
4. Kropf T, “Introduction to Formal Hardware Verification”, Springer Verlag, 2010.
5. UVM Golden Reference Guide, Doulos, 2013.

21LV82 AUDIT COURSE II

vide Automotive Engineering 21AE82

21LV61 PHYSICAL DESIGN LABORATORY

0 0 4 2

- Specification, Design, synthesis and layout design (floorplanning, place and route, power and clock distribution, clock tree synthesis, timing analysis, power analysis, signal integrity, post-layout simulation, back annotation, GDSII generation) of digital building block.

- Specification, Schematic Design, simulation, layout generation, Physical verification (LVS, DRC, RC extraction, post layout simulation, back annotation, GDSII generation) of analog building block.

Total P: 60

21LV62 SYSTEM DESIGN AND VERIFICATION LABORATORY

0 0 4 2

- Partitioning hardware and software modules in system level design
- Hardware Development using Processor Soft Cores and built-in, custom, third party IPs.
- Peripheral Interfacing
- Application Development using Embedded C and Python
- System Integration and Testing

- Coverage based verification
- Assertion based verification
- Features verification using UVM

Total P: 60

21LV63 INDUSTRIAL VISIT AND TECHNICAL SEMINAR

vide Automotive Engineering 21AE63

SEMESTER – III

21LV71 PROJECT WORK – I

vide Automotive Engineering 21AE71

SEMESTER – IV

21LV81 PROJECT WORK – II

Vide Automotive Engineering 21AE81

PROFESSIONAL ELECTIVES THEORY COURSES (Four to be opted)

21LV21 ADVANCED COMPUTER ARCHITECTURE AND PARALLEL PROCESSING

3 0 0 3

PARALLEL PROCESSING MECHANISMS AND MEMORY: Evolution of computer systems. Generation of computer systems – Trends towards parallel processing- Parallel processing mechanisms- parallel computer structure- Architectural classification schemes –Memory and I/O subsystems: Hierarchical Memory structure – Virtual memory system - cache memory management- Memory allocation and management – I/O subsystems (12)

Pipelining: Principles - Classification of pipeline processors - Reservation tables – Interleaved memory organization – Design of arithmetic pipeline – Design of instruction pipeline. Vector Processing: Need – Basic vector processing architecture - Issues in vector processing – Vectorization and optimization methods. (10)

ARRAY PROCESSING: Array processing**:** SIMD Array processors – SIMD interconnection networks – Parallel algorithms for array processors – associative array processing .principles of parallel algorithm design: Design approaches-Design issues-Performance measures and analysis-Complexities-Anomalies in parallel algorithms (11)

MULTIPROCESSOR ARCHITECTURE: Functional structures - Interconnection network – Multi cache problems and solutions – Exploiting concurrency for multiprocessing. Network Computing: Client/Server Systems-clusters (12)

Total L: 45

REFERENCES:

1. Kai Hwang, Naresh Jotwani: Advanced Computer Architecture - Parallelism, Scalability, Programmability, Tata McGraw Hill, 2011.
2. John L Hennessy, “Computer Architecture a Quantitative Approach”, Harcourt Asia Pvt. Ltd., 2011.
3. Seyed Roosta, “Parallel Processing and Parallel Algorithms”, Springer Series, 2000.
4. Hesham El-Rewini, Mostafa Abd-El-Barr, “Advanced Computer Architecture And Parallel Processing”, John Wiley & Sons, 2005.
5. Kai Hwang, “Advanced Computer Architecture: Parallelism, Scalability, Programmability”, Tata McGraw Hill Education, 2003.

21LV22 COMPUTER AIDED DESIGN FOR VLSI SYSTEMS

3 0 0 3

ALGORITHM & SYNTHESIS: VLSI Design cycle - Role of CAD tools in the VLSI Design process -data structures and algorithms: Complexity of algorithms, General purpose methods for combinatorial optimization, logic synthesis – two level synthesis, Binary decision diagrams, and ROBDD principles. (13)

PHYSICAL DESIGN AUTOMATION: Partitioning - KL, FM algorithms, Placement – Simulation based algorithms- Simulated Annealing , Force Directed Algorithm, Partitioning based algorithms- Breuer’s Algorithm, Terminal propagation Algorithm , Cluster Growth Algorithm , Floor planning – slicing floor plan , Constraint Based Floor Planning, Integer Program Based Floor Planning – Pin Assignment. (12)

ROUTING: Grid routing – Maze Routing Algorithms, Global routing - Shortest Path Based Algorithms, Steiner tree based Algorithms, detailed routing – Left Edge algorithm, Dog-Leg Algorithm , Greedy Channel Routing, Switch Box Routing algorithms- over the cell routing, Clock Routing. (10)

LAYOUT SYNTHESIS AND OPTIMIZATION: Layout generation and Optimization of standard cell layout, gate matrix layout and PLA, Layout Compaction – one dimensional and two dimensional compaction. (10)

Total L: 45

REFERENCES:

1. Sherwani N A, “Algorithms for VLSI Physical Design Automation”, Kluwer, 2007.
2. Sait S M and Youssef H, “VLSI Physical Design Automation”, World Scientific, 2004.
3. Sabih H Gerez, “Algorithms for VLSI Design Automation”, John Wiley & Sons, 2008.
4. Micheli G D, “Synthesis and Optimization of Digital Circuits”, Tata McGraw Hill, 2003.
5. Steven M. Rubin, “Computer Aids for VLSI Design”, Addison Wesley, 2nd Edition,1994.

21LV23 ELECTRONIC PACKAGING TECHNOLOGIES

3 0 0 3

OVERVIEW OF ELECTRONIC SYSTEMS PACKAGING: Packaged Electronics – Technologies- Trends- Products and levels of packaging- Packaging aspects of handheld products. (8)

SEMICONDUCTOR PACKAGING: Basics of Semiconductor and Process flowchart; Wafer packaging; Packaging evolution- Chip connection choices -Wire bonding, TAB and flipchip. Single chip packages or modules (SCM)-. Commonly used packages and advanced packages; Materials in packages- Advanced packages - Thermal mismatch in packages; Current trends in packaging- Multichip modules (MCM)-types; System-in package(SIP)- Packaging roadmaps- Hybrid circuits. (14)

ELECTRICAL DESIGN CONSIDERATIONS IN SYSTEMS PACKAGING: Electrical Issues – Resistive Parasitic - Capacitive and Inductive Parasitic- Layout guidelines and the Reflection problem-Interconnection. (12)

THERMAL MANAGEMENT AND RELIABILITY: Heat-transfer fundamentals-. Thermal conductivity and resistance- Conduction, convection and radiation- Cooling –Reliability- Basic concepts- Environmental interactions- Thermal mismatch and fatigue. (11)

Total L: 45

REFERENCES:

1. Rao R Tummala, “Fundamentals of Microsystems Packaging”, McGraw Hill, NY, 2001.
2. William D Brown, “Advanced Electronic Packaging”, IEEE Press, 1999.
3. Tummala, Rao R, “Microelectronics Packaging Handbook”, McGraw Hill, 2008.
4. R.G.Kaduskar and V.B.Baru, “Electronic Product Design”, Wiley India, 2011.
5. Glenn R. Blackwell, “The Electronic Packaging Handbook”, CRC Press, 1999.

21LV24 HARDWARE SECURITY

3 0 0 3

CRYPTOGRAPHIC ALGORITHMS IMPLEMENTATION AND SIDE CHANNEL ANALYSIS: Introduction - Need for hardware security – Basics and vulnerabilities - Design for security - Hardware Implementation of Public-key Cryptographic Algorithm - Private-key Cryptographic Algorithm - Stream Ciphers - Hash Functions – Introduction to Side Channel Analysis - Power Analysis Attack - Timing Attack - Fault Attack - Cache Attack – Scan Chain Based Attack - Design Techniques To Prevent Side Channel Analysis Attacks. (12)

HARDWARE TROJANS: Overview - Nomenclature and Operating Modes - Hardware Trojan Detection Techniques - Logic Testing - Countermeasures - Design Technique - Manufacturing Technique. (11)

PHYSICALLY UNCLONABLE FUNCTIONS: Introduction – Design Approaches - Modeling of PUFs - Sources of Mismatch and Errors - Testing of PUFs - Practical Realizations - Applications. (11)

COUNTERFEIT ICS: Taxonomies - Assessment - Challenges - Detection and Prevention of Recycled ICs - Path Delay Fingerprinting – Secure Hardware Intellectual Properties: - Need for IP protection - Digital Watermarking - Constraint-based Watermarking to Design IP Protection - Watermarking HDL Source Codes by Duplicating Modules. (11)

Total L: 45

REFERENCES:

1. Debdeep Mukhopadhyay, Rajat Subhra Chakraborty, "Hardware Security - Design, Threats, and Safeguards", CRC Press, 2015.
2. Mohammad Tehranipoor, Hassan Salmani, Xuehui Zhang, "Integrated Circuit Authentication Hardware Trojans and Counterfeit Detection", Springer, 2014.
3. Christoph Bohm, Maximilian Hofer, "Physical Unclonable Functions in Theory and Practice", Springer, 2013.
4. Mohammad Tehranipoor, Cliff Wang, "Introduction to Hardware Security and Trust", Springer, 2012.
5. Koc K C, "Cryptographic Engineering", Springer, 2009.

21LV25 LOW POWER VLSI DESIGN

3 0 0 3

POWER DISSIPATION IN CMOS: Physics of Power Dissipation in CMOS FET Devices-Sources of power consumption- -Basic Principles of Low Power Design. SPICE circuit simulation-Gate level Analysis, Architecture level Analysis, Data Correlation Analysis, Monte-Carlo Simulation, Probabilistic Power Analysis. Statistical Techniques - Estimation of Glitching Power - Sensitivity Analysis - Circuit Reliability - Power Estimation at the circuit level - High level Power Estimation - Information Theory based approaches - Estimation of maximum power. (12)

POWER OPTIMISATION TECHNIQUES: Circuit Level – Transistor and Gate Sizing, Equivalent Pin Ordering, Network Restructuring and Reorganization, Special Latches and Flip Flops, Low Power Digital Cell Library, Adjustable Device Threshold Voltage. Leakage current in deep sub micrometer transistors. (11)

SPECIAL TECHNIQUES: Gate Reorganization, Signal Gating, Logic Encoding, State Machine Encoding, Precomputational Logic. Architectural and System Level – Power and Performance Management, Switching Activity Reduction, Parallel Architecture with Voltage Reduction, Flow Graph Transformation. Advanced Techniques- Adiabatic Computation, Pass Transistor Logic Synthesis, Asynchronous Circuits, Low power bus – low swing bus, charge recycling bus, delay balancing. (11)

LOW POWER MEMORIES: Basics of ROM, Low power ROM Technology, Basics of SRAM-Memory Cell-Low Power SRAM Technology-Precharge and Equalization Circuit-Basics of DRAM-Low Power DRAM Technology. Conventional BiCMOS Logic-BiCMOS Logic Family-Low Voltage BiCMOS Logic family-Low Voltage BiCMOS Applications. . (11)

Total L: 45

REFERENCES:

1. Kaushik Roy and Sharat C Prasad ,“Low Power CMOS VLSI circuit Design”, John Wiley and Sons,2000.
2. Kuo J B and Lou J H, “Low Voltage CMOS VLSI Circuits”, John Wiley and Sons, Singapore, 1999.
3. Gary B Yeap K, "Practical Low Power Digital VLSI Design”, Kluwer Academic Publishers, 1998.
4. Abdelatif Belaouar, Mohamed I Elmasry,"Low Power Digital VLSI Design", Kluwer Academic Press, 1995.
5. Anantha P Chandrakasan and Robert W Brodersen, “Low Power Digital CMOS Design”, Kluwer Academic Publishers, Holland, 1995.

21LV26 SEMICONDUCTOR MEMORY DESIGN

3 0 0 3

RANDOM ACCESS MEMORY TECHNOLOGIES: Static Random Access Memories (SRAM): SRAM cell structures, MOS SRAM Architecture, MOS SRAM cell and peripheral Circuit Operation, SOI Technology, Advanced SRAM Architectures and Technologies, Application Specific SRAMs. Dynamic Random Access Memories (DRAM): DRAM Technology Development, CMOS DRAM, DRAM cell theory and advanced cell structures, BiCMOS DRAM, soft error failures in DRAM, Advanced DRAM Design and Architecture, Application Specific DRAM. (11)

NON-VOLATILE MEMORIES: Masked ROM, High Density ROMs, Programmable ROM, Bipolar ROMs, CMOS PROMs, Erasable(UV) Programmable ROM(EPROM), Floating Gate EPROM Cell, One time Programmable EPROM (OTPEPROM), Electrically Erasable PROMS, EEPROM Technology and Architecture, Non volatile SRAM, Flash Memories (EPROM or EEPROM), Advanced Flash Memory Architecture. (12)

SEMICONDUCTOR MEMORY RELIABILITY AND RADIATION EFFECTS: General Reliability Issues-RAM Failure Modes and Mechanism-Nonvolatile Memory Reliability. Radiation Effects- Radiation Hardening Techniques-Radiation Hardening Process and Design Issues-Radiation Hardened Memory Characteristics. (11)

ADVANCED MEMORY TECHNOLOGIES : Ferroelectric Random Access Memories (FRAMs)-Analog Memories-Magnetoresistive Random Access Memories (MRAMs)-Experimental Memory Devices. Memory Hybrids and MCMs (2D)-Memory Stacks and MCMs (3D)-Memory MCM Testing and Reliability Issues. (11)

Total L: 45

REFERENCES:

1. Ashok K Sharma, “Semiconductor Memories Technology, Testing and Reliability”, Wiley, 2002.
2. Ashok K Sharma, “Advanced Semiconductor Memories – Architecture, Design and Applications, Wiley, 2002.
3. Betty Prince, "Emerging Memories - Technologies and Trends", Kluwer Academic Publishers, 2002.
4. Kiyooltoh, Masashi Horiguchi and Hitoshi Tanaka, "Ultra-Low Voltage Nano-Scale Memories", Springer, 2007.
5. Jesse Russell and Ronald Cohn, "Content-Addressable Memory", Bookvika Publishing, 2012.

21LV27 / 21LC35 / 21LW38 SYSTEM ON CHIP DESIGN

3 0 0 3

INTRODUCTION: Components of SoC - Design flow - Driving factors for hardware-software codesign, design space, system specification and modeling- Hardware Software tradeoffs- Co-Design Approaches, System Design Methodologies - Models of Computation- Platform based SoC design - Processor Selection -Concepts in Processor Architecture: Instruction set architecture (ISA) - Soft and Firm processors, Custom-Designed processors- on-chip memory - Prototyping and emulation. (11)

COMMUNICATION ARCHITECTURES: On-chip Buses: Characteristics - Data Transfer Modes - Bus Topology Types - Standard on-chip bus-based communication architectures: AMBA, CoreConnect, STBus, SMART Interconnect, Wishbone, and Avalon - Socket-based on-chip bus interface standards: Open Core Protocol, virtual component interface, and device transaction level - Network-on-chip - Network Topology - Switching Strategies - Routing Algorithms - Flow Control - NoC Architectures - Off-chip bus architecture standards. (12)

IMPLEMENTATION AND TESTING: System synthesis - Transaction Level Modeling (TLM) based design - Software synthesis - Hardware synthesis - IP based system design: Types of IP, IP Generation - HDL based IPs, Model based IPs and High Level Language based IPs - IP Sources - Built-in IPs, Custom IPs and Third Party IPs. - Real-time operating system (RTOS) - Peripheral Interfacing and Programming - SOC TESTING: Manufacturing test of SoC: Core layer, system layer, application layer-P1500 Wrapper Standardization-SoC Test Automation (STAT). (12)

APPLICATIONS: Automotive - Communications - Defense and Aerospace - Robotics, Control and Instrumentation - Image and Video Processing - Artificial Intelligence - Medical - High Performance Computing - Dynamic System-on-chip. (10)

Total L: 45

REFERENCES:

1. Patrick Schaumont “A Practical Introduction to Hardware/Software Co-design”, Patrick Schaumont, 2nd Edition, Springer, 2012.
2. Michael J Flynn and Wayne Luk, “Computer system Design: System-on-Chip”, Wiley-India, 2012.
3. Sudeep Pasricha and Nikil Dutt, “On Chip Communication Architectures: System on Chip Interconnect”, Morghan Kaufmann Publishers, 2008.
4. Wang, Wu and Wen, “VLSI Test Principles and Architectures”, Morgan Kaufmann, 2006.
5. Daniel D. Gajski, Samar Abdi, Andreas Gerstlauer and Gunar Schirner, "Embedded System Design : Modeling, Synthesis and Verification", Springer, 2009.

21LV28 VLSI FOR IOT SYSTEMS

3 0 0 3

INTRODUCTION: Concept of connected world – Need, Legacy systems for connected world – features and limitations, Key features of IoT architecture, Merits and Demerits of IoT technology, Applications driven by IoT technology – examples (9)

COMPONENTS OF IOT: Review of classic embedded system architecture, Basic building blocks of an IoT system –Sensors, Actuators, Computing nodes and Connectivity. Sensors used in IoT systems – Characteristics and requirements, Types of sensors for IoT systems, Compute nodes of IoT, Connectivity technologies in IoT – Software in IoT systems- Embedded Programming.. (12)

IC TECHNOLOGY FOR IOT: SoC architecture for IoT Devices– Application Processors, Microcontrollers, Smart Analog; Memory architecture for IoT – Non Volatile Memories (NVM), Embedded Non-Volatile Memories, Anti-Fuse One Time Programmable (OTP) memories, Power Management - Low Drop Out Regulators, DC-to-DC Converters, Voltage References, Power Management Units (PMUs) in IC’s and Systems, FPGA in IoT systems. (12)

ELECTRONIC SYSTEM DESIGN FOR IOT: Requirements, Designing Computing blocks in IoT systems. System Power Supply Design for IoT systems, Mixed Signal challenges in hardware systems, Form Factor – Guidelines and prevailing standards. Component models & System Design – Feasibility and challenges, System Level Integration, Operating conditions of IoT devices and impact on Electronic System Design; Hardware Security issues, EMI/EMC, SI/PI and Reliability Analysis in IoT systems. (12)

Total L: 45

REFERENCES:

1. Alioto, “Enabling the Internet of Things- From Integrated Circuits to Integrated Systems”, Springer Publications, First Edition, 2017.
2. Pieter Harpe, Kofi A. A. Makinwa, Andrea Baschirotto, "Hybrid ADCs, Smart Sensors for the IoT, and Sub-1V & Advanced Node Analog Circuit Design”, Springer International Publishing AG, 2017.
3. Jim Lipman, Sidense Corp.” NVM memory: A Critical Design Consideration for IoT Applications”- https://www.design reuse.com/articles/32614/nvm-memory-iot-applications.html.
4. ApekMulay, “Sustaining Moore’s Law: Uncertainty Leading to a Certainty of IoT Revolution” Morgan and Claypool Publishers, 2015.
5. Rashid Khan, Kajari Ghoshdastidar, Ajith Vasudevan, “Learning IoT with Particle Photon and Electron”, Packt Publishing Limited (Verlag), 2016.

21LV29 VLSI SIGNAL PROCESSING

3 0 0 3

REALIZATION OF DIGITAL FILTERS: FIR filter design - IIR filter design - Direct form I, II, Cascade, parallel, Ladder - Lattice filters. (11)

ITERATION BOUND: Introduction, Data flow graph representations, loop bound and iteration bound, Algorithms for computing Iteration bound, iteration Bound of multirate Data - Flow Graphs. PIPELINING AND PARALLEL PROCESSING: Introduction - Pipelining of FIR Digital filters - Parallel processing - Pipelining and parallel processing for Low power. (11)

TRANSFORMATIONS: RETIMING**:** Introduction - Definitions and Properties - Solving system of Inequalities - Retiming Techniques. UNFOLDING: Introduction - An algorithm for unfolding - Properties of unfolding - Critical path, unfolding and retiming - Application of unfolding. FOLDING: Introduction - folding Transformation - Register Minimization Techniques - Register Minimization in folded Architectures. (11)

FAST CONVOLUTION: Cook-Toom algorithm – modified Cook-Toom algorithm Winograd algorithm- modified Winograd algorithm, Algorithmic strength reduction in filters and transforms-parallel FIR filters, Parallel architectures for Rank-order filter. (12)

Total L: 45

REFERENCES:

1. Keshab K Parhi, “VLSI Digital Signal Processing Systems Design and Implementation”, Wiley - Inter science, 2007.
2. John G Proakis and Dimitris G Manolakis, “Digital signal processing – Principles, Algorithms and Applications” Pearson, 2014.
3. Uwe Meyer Baese, “Digital Signal Processing with Field Programmable Gate Arrays”, Springer, 2014.
4. Lonnie C Ludeman, “Fundamentals of Digital Signal Processing”, Wiley India (P) Ltd., 2010.
5. Peter Pirsch “Architectures for Digital Signal Processing”, Wiley India (P) Ltd., 2009.

21LV38 CURRENT MODE ANALOG SIGNAL PROCESSING

3 0 0 3

CURRENT MODE CIRCUIT BUILDING BLOCK: Current-mode vs. voltage mode processing; Trans linear circuits, supply-current sensing, current conveyors, current mode instrumentation amplifiers and precision rectifiers. (12)

CURRENT MODE OPERATIONAL AMPLIFIERS: Dynamic current mirrors, High-performance amplifier architectures. current-feedback operational amplifiers, High frequency CMOS Transconductors. (11)

CURRENT MODE FILTERS: switched current processing, trans linear/log domain filters, switched-current Integrators, Switched -current filters. (11)

CURRENT MODE DATA CONVERTERS: Current mode DAC and ADC characteristics, Current Mode A/D Converters: Active mirror, Current matching; Current Mode D/A Converters: Weighted current Source, High Speed current switch. (11)

Total L: 45

REFERENCES:

1. C. Ioumazou, F.J. Lidgey and D.G. Haigh, “Analog IC Design : the Current Mode Approach", IEE, Peter Peregrinus 1993.
2. Leila Safari , Giuseppe Ferri , Shahram Minaei , Vincenzo Stornelli, “Current-Mode instrumentation Amplifiers (Analog Circuits and Signal Processing)”, Springer; 2019.
3. Benhard Razavi, “Data Converters”, Kluwer Publishers, 2005.
4. Jacob Baker, “CMOS, Circuit Design Layout and Simulation”, Wiley- IEEE Press, 2011.
5. Yuan, Fei, "CMOS Current-Mode Circuits for Data Communications”,-1st Edition Springer US,2007

21LV30 HIGH SPEED DIGITAL DESIGN

3 0 0 3

TRANSMISSION LINES AND CROSSTALK: Transmission line structures, signal propagation, transmission line parameters, line impedance, propagation delay, Transmission line reflections, Cross talk- Mutual inductance, Mutual capacitance, cross talk induced noise, minimizing cross talk. (14)

INTERCONNECTS AND POWER DISTRIBUTION: Interconnect technologies, Multilevel multilayer interconnects, propagation delay, crosstalk analysis. Power Distribution - losses, the need for low-impedance planes and decoupling capacitors and their selection. (10)

CLOCK DISTRIBUTION AND TIMING: High-quality clock signals to components, boards, and systems, Common clock timing and source synchronous timing. (10)

ELECTROMAGNETIC COMPATIBILITY (EMC) AND GROUNDING: Designing for EMC, EMC regulations, typical noise path, methods of noise coupling, and methods of reducing interference in systems, Safety grounds ,signal grounds, single-point

ground systems, multi-point ground systems, hybrid grounds, functional ground layout, practical low frequency grounding, hardware grounds, grounding of cable shields, ground loops, shield grounding at high frequencies. (11)

Total L: 45

REFERENCES:

1. Howard Johnson, Martin Graham, "High speed Digital design", Pearson, 2005.
2. HallS, HallG and McCallJ, " High speed digital system design: A Handbook of Interconnect theory and practices", Wiley Interscience,2000
3. Hartmut Grabinski, " Interconnects in VLSI design", Kluwer,2000
4. GoelAK, "High speed vlsi interconnections" ,Wiley 2007
5. BogatinE, "Signal integrity-simplified", Prentice Hall ,2003.

21LV31 MIXED SIGNAL VLSI DESIGN

3 0 0 3

SWITCHED CAPACITOR C FILTERS: Universal active filter (KHN), Switched capacitor filters: Switched capacitor resistors - Integrator- amplifiers – comparators - sample & hold circuits –- Biquad. (11)

CONTINUOUS TIME FILTERS: Introduction to Gm - C filters - CMOS Transconductors using Triode transistors, active transistors - BiCMOS transconductors – MOSFET C Filters - Tuning Circuitry - Dynamic range performance - Elementary transconductor building block- First and Second order filters. (11)

DIGITAL TO ANALOG & ANALOG TO DIGITAL CONVERTERS: Non-idealities in the DAC - Nyquist rate DAC's: Charge redistribution, Hybrid, segmented DAC's - Techniques for improving linearity - Non-idealities in the ADC, High Speed ADC's: Flash, pipelined, folding ADC's. SIGMA DELTA CONVERTERS**:** Over sampled converters - over sampling without noise & with noise - implementation imperfections - first order modulator - decimation filters - second order modulator - sigma delta DAC & ADC's. ADC and DAC testing methods. (12)

ANALOG AND MIXED SIGNAL EXTENSIONS TO HDL: Introduction - Language design objectives - Tolerance groups - Conservative systems - Time and the simulation cycle - A/D and D/A Interaction - Quiescent Point - Frequency domain modeling and examples. Analog extensions to Verilog**:** Introduction - data types –Expressions – Signals - Analog behavior – Hierarchical Structures – Mixed signal Interaction. (11)

Total L: 45

REFERENCES:

1. Phillip Allen and Douglas Holberg "CMOS Analog Circuit Design", Oxford University Press, 2012.
2. Jacob Baker, "CMOS, Circuit Design Layout and Simulation", Wiley- IEEE Press, 2011.
3. David A Johns and Ken Martin, "Analog Integrated Circuit Design", John Wiley and Sons, 2008.
4. Benhard Razavi, "Data Converters", Kluwer Publishers, 2005.
5. Kenneth S Kundert and Olaf Zinke, "The Designers Guide to Verilog AMS", Kluwer Publications, 2004.

21LV32 RF CIRCUIT DESIGN

3 0 0 3

PASSIVE RF COMPONENTS AND TRANSMISSION LINE ANALYSIS: High frequency Resistors, Capacitor and Inductors – Transmission Line Analysis: Line equation, Micro strip line, Voltage Reflection Co-efficient, propagation constant phase velocity and special termination - Smith Chart-Impedance transformation - Analysis of parallel RL circuit and parallel RC circuit. (9)

SINGLE AND MULTI PORT NETWORK THEORY AND RF FILTER DESIGN: Definition - properties - interconnection of networks - ABCD parameters and S parameters - RF Filter Resonator and filter configuration - Butterworth and chebyshev filters. Design of micro strip filters. (9)

DESIGN OF MATCHING NETWORK: Matching by Discrete Components - Design of two-component matching network, Design of T and π matching network- Matching by micro strip line - Design of matching network - Design of stub matching. (9)

RF ACTIVE COMPONENTS, THEIR MODELING AND RF AMPLIFIER DESIGN: Components: RF Diode: PIN diode and Gunn Diode. RF Bipolar junction Transistor, RF field effect transistor - Modeling: Diode model, Transistor model, and FET model – RF Amplifier: Characteristics, power relations and Stability considerations. (9)

RF OSCILLATOR AND MIXER DESIGN: Basic oscillator model - Design of fixed frequency oscillator - Dielectric resonator oscillator - voltage controlled oscillator - gun element oscillator - Basic concepts - Design of single ended mixer- Double ended mixer. (9)

Total L: 45

REFERENCES:

1. Razavi B, "RF Micro Electronics", Prentice Hall PTR, 2011.
2. Reinhold Ludwig and Pavel Bretchko, "RF Circuit Design", Pearson Education Asia Publication, 2011.

3. Peter P Kenington, “High Linearity RF Amplifier Design”, Artech House, 2007.
4. Lee T H, “The Design of CMOS Radio Frequency Integrated Circuits”, Cambridge University Press, 2004.
5. Matthew M Radmanesh, “Radio Frequency and Microwave Electronics Illustrated”, Pearson Education, Asia Publication, 2001.

21LV33 / 21LW40 VLSI FOR WIRELESS COMMUNICATION

3 0 0 3

OVERVIEW OF MODULATION SCHEMES: Classical Channel - Wireless Channel Description - Path Loss - Channel Model and Envelope Fading - Multipath Fading: Frequency Selective and Fast Fading - Summary of Standard Translation. (10)

RECEIVER FRONT END: Filter Design - Rest of Receiver Front End: Non idealities and Design Parameters - Nonlinearity – Noise - Noise Figure. AMPLIFIER DESIGN: Low Noise Amplifier Design - Wideband LNA - Narrowband LNA - Impedance Matching - Automatic Gain Control Amplifiers – Power Amplifiers. (13)

MIXERS: Balancing Mixer: Qualitative Description of the Gilbert Mixer - Conversion Gain – Distortion -Noise -Analysis of Gilbert Mixer: Low Frequency Case and High-Frequency Case – A Complete Active Mixer. Unbalanced Switching Mixer - Conversion Gain- Distortion - Noise - A Practical Unbalanced Switching Mixer. Single ended Sampling Mixer - Conversion Gain - Distortion - Intrinsic Noise - Extrinsic Noise - Demodulators. (11)

FREQUENCY SYNTHESIZERS: Phase Locked Loops - Phase Detector – Analog Phase Detectors – Digital Phase Detectors - Voltage Controlled Oscillators - Frequency Dividers - LC Oscillators - Ring Oscillators - Phase Noise - A Complete Synthesizer Design Example (DECT Application). Loop filter: Voltage Controlled Oscillators - Design Approaches. (11)

Total L: 45

REFERENCES:

1. Bosco H Leung “VLSI for Wireless Communication”, Pearson Education, 2002.
2. Emad N Farag and Mohamed I Elmasry, “Mixed Signal VLSI Wireless Design - Circuits and Systems”, Kluwer Academic Publishers, 2000.
3. laskar J, Matinpourand B and Charaborty S, “Modern receiver front ends: Systems, Circuits and integration”, Wiley 2004
4. Leenearts D, Vander J Tang and Vaucher C S, “Circuit design for RF transceivers”, Springer 2002.
5. Luzzatto A and Shirazi G, “Wireless Transceiver Design: Mastering the Design of Modern Wireless Equipment and Systems”, Wiley 2007.

21LV34 MODELLING AND SIMULATION OF NANOSCALE TRANSISTORS

3 0 0 3

ANALYTICAL MODELLING: Introduction - Types of Models - Attributes of Good Compact Models - Model Formulation - Model Implementation in Circuit Simulators - Model Testing - Parameter Extraction - Simulation and Extraction for RF Applications. Analytical Solution Methods: Parabolic Approximation - Variable Separable - Numerical Simulation - Fourier series - Green Function - Bessel Function. (10)

TECHNOLOGY-ORIENTED CAD & DEVICE CAD: Introduction – Process and Device CAD – Process Simulation Techniques – Interfaces in process and Device CAD – CMOS Technology - Ion Implantation – Oxidation – Impurity Diffusion. DEVICE CAD: Semiconductor Device Analysis – The pn Junction – Equilibrium Conditions – Non-equilibrium Conditions - Bipolar Junction Structures - Carrier Densities – Carrier Transport and Conversation - Field-Effect Structures. The MOS capacitor – Basic MOSFET I-V Characteristics – Threshold Voltage in Nonuniform Substrate – MOS Device Design by Simulation. (13)

TCAD SIMULATION: Process simulator – Device simulator – Advanced concepts – drift-diffusion, hydrodynamic model, stress models - Structure editor - meshing concepts - work bench – Plotting – Scripting -Monte-carlo simulation - Electromagnetic simulation. (11)

NOVEL TRANSISTOR ARCHITECTURES: Nanowire transistor - High electron mobility transistor - Tunnel field effect transistor - Single electron transistor - Carbon nanotube transistor - Double gate and multi gate MOS transistor - Electron wave transistor - Electron spin transistor. (11)

Total L: 45

REFERENCES:

1. Robert W. Dutton and Zhiping Yu, “Technology CAD Computer Simulation of Processes and Devices”, Springer, 2012.
2. Rainer Waser, “Nanoelectronics and Information Technology: Advanced Electronic Materials and Novel Devices”, 3rd Edition, Wiley VCH Verlag, Weiheim, 2012.
3. Yannis Tsividis and Colin McAndrew, "Operation and Modeling of the MOS Transistor", 3rd Edition, Oxford University Press, 2011.
4. Mark S. Lundstrom and Jing Guo, "Nanoscale Transistors: Device Physics, Modeling and Simulation", Springer, 2006.
5. Shunri Oda and David Ferry, “Silicon Nanoelectronics”, CRC Press, New York, 2005.

21LV35 NANOSCALE DEVICES

3 0 0 3

OVERVIEW: Nano devices, Nano materials, Nano characterization-Definition of Technology node. Basic CMOS Process flow-MOS Scaling theory, Issues in scaling. MOS transistors: Short channel effects, Description of a typical 65 nm CMOS technology- Requirements for Non classical MOS transistor. MOS CAPACITOR: Role of interface quality and related process techniques, Gate oxide thickness scaling trend, SiO2 vs High-k gate dielectrics- Integration issues of high-k -Interface states, bulk charge, band offset, stability, reliability - Q_{bd} high field, possible candidates, CV and IV techniques. (11)

METAL GATE TRANSISTOR : Motivation, requirements, Integration Issues- Transport in Nano MOSFET, velocity saturation, ballistic transport, injection velocity, velocity overshoot - Ultrathin body SOI - double gate transistors, integration issues - Vertical transistors - FinFET and Surround gate FET (11)

METAL SOURCE/DRAIN JUNCTIONS: Properties of Schotky junctions on Silicon, Germanium and compound semiconductors -Work function pinning- Germanium Nano MOSFETs: strain, quantization, Advantages of Germanium over Silicon, PMOS versus NMOS. Compound semiconductors - material properties, MESFETs Compound semiconductors MOSFETs in the context of channel quantization and strain, Hetero structure MOSFETs exploiting novel materials, strain, and quantization. (11)

SYNTHESIS OF NANOMATERIALS: CVD, Nucleation and Growth, ALD, Epitaxy, MBE. Compound semiconductor hetero-structure growth and characterization - Quantum wells and Thickness measurement techniques - Contact - step height, Optical - reflectance and ellipsometry.AFM. Characterization techniques for nanomaterials: FTIR, XRD, AFM, SEM, TEM, EDAX etc-Applications and interpretation of results. Emerging Nanomaterials - Carbon Nanotubes, nanorods and other nano structures, LB technique, Soft lithography etc. Microwave assisted synthesis, Self assembly etc. (12)

Total L: 45

REFERENCES:

1. Karl Goser, Nanoelectronics and Nanosystems: From Transistors to Molecular and Quantum Devices, Springer, 2005.
2. WaserRanier, “Nanoelectronics and Information Technology (Advanced Electronic Materials and Novel Devices”, Wiley-VCH, 2005.
3. Khurshed Ahmad Shah, Farooq Ahmad Khanday , “Nanoscale Electronic Devices and Their Applications”, 1st Edition, CRC Press, August 2020.
4. Chao Huang, “Robust Computing with Nano-scale Devices: Progresses and Challenges” (Lecture Notes in Electrical Engineering Book 58) 2010.
5. Vinod Kumar Khanna , "Integrated Nanoelectronics, Nanoscale CMOS, Post-CMOS and Allied Nanotechnologies", Springer Publication, 2016.

21LV39 QUANTUM CIRCUIT DESIGN

3 0 0 3

INTRODUCTION: Quantum Computation vs Classical Computation - Mathematics and Quantum Mechanics Preliminaries - Linear Algebra - Unitary Matrices - Tensor Product - Pauli Matrices - Notions of Quantum Information - Quantum state - Dirac Notation - Superpostition - Entanglement - Bell State - Probabilities and Measurements. (12)

QUANTUM GATES AND CIRCUITS: Qubits - Quantum Gates - Single Qubit Gates - Multiple Qubit Gates - Quantum Gates Acting on One Qubit - Bloch sphere Representation - Circuit Models - Design of Quantum Circuits. (11)

QUANTUM ALGORITHM AND IMPLEMENTATION: Deutsch’s Algorithm - Deutsch-Jozsa Algorithm - Bernstein-Vazirani Algorithm - Quantum Fourier Transform - Shor's Factoring Algorithm - Grover's Search Algorithm - Quantum error correction - Fault-tolerant Computation - Computational Complexity. (12)

QUANTUM CRYPTOGRAPHY: No Cloning Theorem - Private Key Cryptography - Quantum Key Distribution - BB84 protocol - B92 protocol - EPR protocol - Secured Quantum Key Distribution - Post Quantum Cryptography. (10)

Total L: 45

REFERENCES:

1. Michael A Nielsen and Isaac L Chuang, “Quantum Computation and Quantum Information”, Cambridge University Press, 2010.
2. Phillip Kaye, Raymond Laflamme and Michele Mosca, "An Introduction to Quantum Computing", Oxford University Press, 2007.
3. Eleanor Rieffel and Wolfgang Polak, "Quantum Computing A Gentle Introduction", The MIT Press, 2011.
4. George F Viamontes, Igor L Markov and John P Hayes, "Quantum Circuit Simulation", Springer, 2009.
5. Chris Bernhardt, "Quantum Computing for Everyone", The MIT Press, 2019.

21LV36 QUANTUM DOT CELLULAR AUTOMATA NANOTECHNOLOGY

3 0 0 3

Introduction: Emerging Nanotechnologies- Electronics beyond Moore's law - Limitations of CMOS technology- Alternatives to MOSFET and Challenges - Emerging Transistor Based Devices-IC Technology beyond CMOS Era- USDM and Quantum computing- QCA modeling approach. (11)

QCA Terminology: QCA Basics - Schrödinger's equation in quantum wires - Quantum boxes - Non-zero angular momentum states- Spherical quantum dots -Tiny quantum dots- Cuboidal dots- Dots of arbitrary shape -Approaches to pyramidal dots- Matrix approaches-Transport through dot arrays- Crossovers in QCA -Convergence tests- Efficiency- Tool for QCA Simulation. (11)

Design of Digital circuits in QCA: Logic Primitives in QCA- Clocking in QCA - Role and Types -Design of Logic Gates and Multiplexer in QCA - Design of a One-Bit Full-Adder - Flip-Flop in QCA - Design ofRipple Carry Adder (RCA) and Prefix Adders in QCA- Design of 16-Bit Hybrid Adder in QCA- Layout Level Implementation of adders and Comparisons. Introduction to Multipliers -Design of a Multiplier in QCA - The Baugh - Wooley Multiplier for 2's Complement Numbers- Design of Baugh-Wooley Multiplier in QCA. (12)

Transform in QCA: Discrete Hadamard Transform Computation in QCA - Basics of Discrete Hadamard Transform-Mathematical Formulation for DHT Computation- QCA Realization - Performance of a Full-Parallel Addition Strategy - Applications of Quantum Dot Cellular Automata Technology. (11)

Total L: 45

REFERENCES:

1. K. Sridharan, Vikramkumar Pudi, "Design of Arithmetic Circuits in Quantum Dot Cellular Automata Nanotechnology", Studies in Computational Intelligence, Springer International Publishing, 2015.
2. Fabrizio Lombardi, Jing Huang, "Design and Test of Digital Circuits by Quantum-Dot Cellular Automata", Artech House, 2007.
3. Kasper, E., Paul, D, "Silicon Quantum Integrated Circuits -Silicon-Germanium Heterostructure Devices: Basics and Realisations", Springer-Verlag Berlin Heidelberg, 2005.
4. Paul Harrison, Alex Valavanis, "Quantum Wells, Wires and Dots: Theoretical and Computational Physics of Semiconductor Nanostructures", 4th Edition, Wiley, 2016.
5. Anand Mohan, Ashutosh Kumar Singh, and Trailokya Nath Sasamal, "Quantum-Dot Cellular Automata Based Digital Logic Circuits: A Design Perspective", Springer Nature, 2019

21LV37 VLSI TECHNOLOGY

3 0 0 3

MATERIAL PROPERTIES & CRYSTAL GROWTH: Crystal structure- axes & planes, Crystal defects-Point defects & dislocations Crystal growth- Bridgman, Czochralski techniques & Zone process, Doping in the melt. DIFFUSION & ION IMPLANTATION: Nature of diffusion-interstitial, Substitutional, interstitial substitutional movements, Diffusion constant, Dissociate process, Diffusion equation- D is constant & function, Diffusion systems, problems in Si Diffusion, Evaluation Techniques Ion Implantation: Penetration range, Implantation Damage, Annealing, Implantation Systems. (12)

OXIDATION & EPITAXY OXIDATION: Thermal Oxidation-Intrinsic, Extrinsic silicon Glass, Oxide formation, Kinetics of Oxide growth, Oxidation systems, Faults, Anodic Oxidation. EPITAXY: Vapour Phase Epitaxy (VPE)- transport, reaction and growth, Chemistry of growth, Insitu etching, Selective epitaxy, imperfections, Liquid Phase Epitaxy, LPE system, Evaluation of epitaxial layers. (11)

ETCHING & LITHOGRAPHY:LITHOGRAPHY: Pattern generation & Masking, Printing & Engraving-Optical, E-Beam, ion Beam, X-Ray, Photo resists, Defects. ETCHING: Wet chemical etching- anisotropic etchants, Etching for non-crystalline films-Plasma etching, Plasma-assisted etching, cleaning. (11)

DEVICE & CIRCUIT FABRICATION: Isolation- Mesa, Oxide, PN-junction isolations, Self Alignment, Local Oxidation, Planarization, Metallization and Packaging. Circuits – N, P and CMOS Transistors, Memory devices, BJT Circuits – Buried Layer, PNP and NPN Transistors, Diodes, Resistors, Capacitors. (11)

Total L: 45

REFERENCES:

1. Sorab K Gandhi, "VLSI Fabrication Principles – Silicon and Gallium Arsenide", Wiley Interscience Publications, New York 2008.
2. Sze S M,"VLSI Technology", McGraw Hill, New York, second edition,2017.
3. Chang S Y and Sze S M, "ULSI Technology", McGraw Hill, New York, 2007.
4. Donald Neamen,DhrubesBiswas, " Semiconductor Physics and Devices"McGraw Hill, New York,Fourth edition,2017.
5. Sze S M and KwokKNg ,"Physics of Semiconductor Devices", John Wiley , 2006

OPEN ELECTIVES THEORY COURSES

21LC91 / 21LW91 / 21LV91 / 21LN91 SMART CITIES

3 0 0 3

SMART CITIES: Ideal Smart City loop, Socio-economic and environmental issues, Implications of Urbanization, Urbanization models and global trends, Urbanization in India, Criteria for smart cities, Smartness - Citizens, Living, Environment, Mobility, Economy, Governance Pillars of Smart cities, Buildings, Utilities, Smart Energy,Transportation and road Infrastructure, Health Care, Stakeholders' perceptions, Sustainability issues (12)

FUNDAMENTAL TECHNOLOGIES AND OPPORTUNITIES: Ubiquitous computing, Big Data, Networking, Internet of Things, Cloud computing, Service-oriented architectures, Cyber security architectures. Opportunities: Smart street lighting, Smart Parking, Environmental pollution monitoring, Vehicular tracking, Smart Traffic Control, Waste Management, Smart Grid, Amenity availability, Heritage Information portal, Mobile application design, development and Visualization. (12)

ICT FOR SMART CITIES: Complex Urban systems ICT Infrastructure modeling, Typical Edge Environment, Smart Cities as Systems of Systems, IoT Centric approach, IoT Protocols: WiFi, 6LowPAN, Cellular, NFC, LoRa, NBIOT (11)

CASE STUDIES OF SMART CITIES: European Smart cities, Singapore, Taipei and Surabaya, Mumbai and New Delhi. Smart Village Clusters and Urbanization: Application of smart city Concepts (10)

Total L: 45

REFERENCES:

1. Carlo Ratti and Matthew Claudel, “The City of Tomorrow: Sensors, Networks, Hackers, andthe Future of Urban Life (The Future Series)”, Yale University Press 2016.
2. Stephen Goldsmith, Susan Crawford, “The Responsive City: Engaging CommunitiesThrough Data-Smart Governance”, 1st Edition Jossey Bass – Wiley, 2014.
3. Anilkumar ,”Introduction to Smart Cities”,Pearson India Education series Pvt Ltd, 2020.
4. Sameer Sharma ,”Smart cities Unbounded - Ideas and Practices of Smart cities in India”,BloomsburyPublishing India Pvt Ltd, 2018.

21LC92 / 21LW92 / 21LV92 / 21LN92 RADIATION HAZARDS

3 0 0 3

BIOLOGICAL EFECTS OF RADIATION AND PROTECTION: Production and properties - interaction mechanism of RF and mircrowaves with biological systems: Thermal and non-thermal effects on whole body, lens and cardiovascular systems -tissue characterization and Hyperthermia and other applications-Biomagnetism - Effects - applications. (9)

NON IONIZONG RADIATION: Historical context- Extent of the problem-Understanding non-ionising EMR- Units of measurement –The impact of non-ionising EMR on the body- Legislation- Extra Low Frequency Radiation- Definition and use- Health effects- Risk management- Radio Frequency Radiation- Infra Red Radiation- Visible Light-Ultraviolet -Legislation - Implications for practice. (12)

RF AND MICROWAVE RADIATION: Introduction - Sources of radio frequency radiation- Effects of radio frequency radiation- The development of standards for human safety- The calculation of RF field quantities- Microwave antenna calculations and safety with moving microwave beams - Other antenna system calculations -Simultaneous irradiations and peak pulse power limits -Mobile communications systems. (12)

RF RADIATION MEASUREMENTS AND METHODS: Radiation measurements and methods- X-rays and X-ray measuring instruments - Planning surveys and measurements - Conducting radiation measurements and surveys Leakage surveys - Exposure measurements -Designing to reduce radiation hazards - Radio frequency radiation safety management and training. (12)

Total L : 45

REFERENCES :

1. Ronald Kitchen,”RF Microwave Radiation Safety Handbook”, Newness, Second Edition, 2001.
2. Thomas S. Curry, James E. Dowdey and Robert E. Murry, “Christensen's Physics of Diagnostic Radiology”, Lea & Febiger,U.S.Fourth Edition, Reprint 2010.
3. Harry Moseley, Hospital Physicists' Association, Non-ionising radiation: microwaves, ultraviolet, and laser radiation, A. Hilger, in collaboration with the Hospital Physicists' Association, 1988.