13.Courses of Study and Scheme of Assessment

ME VLSI DESIGN **(2021 REGULATIONS)**

(Minimum No. of credits to be earned: 70*)

Course Code	Course Title	Hours/Week			Credits	Maximum Marks			CAT
		Lecture	Tutorial	Practical		CA	FE	Total	
I SEMESTER									
21LV01	Graph Theory and Optimization Techniques	3	1	0	4	50	50	100	PC
21LV02	Designing with FPGAs	2	2	0	4	50	50	100	PC
21LV03	Device Modelling	3	0	0	3	50	50	100	PC
21LV04	Digital IC Design	3	0	0	3	50	50	100	PC
21LV05	VLSI Testing	3	1	0	4	50	50	100	PC
21LV06	Research Methodology and IPR	2	0	0	2	50	50	100	RMC
21LV72	Audit Course – I	2	0	0	Grade	100	0	100	MC
21LV51	Scripting and SystemVerilog Laboratory	0	0	4	2	50	50	100	PC
21LV52	Microelectronics Simulation Laboratory	0	0	4	2	50	50	100	PC
Total 30 hrs		**18**	**4**	**8**	**24**	**500**	**400**	**900**	
II SEMESTER									
21LV07	Analog VLSI Circuits	3	1	0	4	50	50	100	PC
21LV08	Hardware Verification Techniques	3	0	0	3	50	50	100	PC
21LV__	Professional Elective – I	3	0	0	3	50	50	100	PE
21LV__	Professional Elective – II	3	0	0	3	50	50	100	PE
21LV__	Professional Elective – III	3	0	0	3	50	50	100	PE
21LV82	Audit Course – II	2	0	0	Grade	100	0	100	MC
21LV61	Physical Design Laboratory	0	0	4	2	50	50	100	PC
21LV62	System Design and Verification Laboratory	0	0	4	2	50	50	100	PC
21LV63	Industrial Visit and Technical Seminar	0	0	4	2	50	50	100	EEC
Total 30 hrs		**17**	**1**	**12**	**22**	**500**	**400**	**900**	
III SEMESTER									
21LV__	Professional Elective – IV	3	0	0	3	50	50	100	PE
21LV__	Open Elective	3	0	0	3	50	50	100	OE
21LV71	Project Work I	0	0	12	6	50	50	100	EEC
Total 18 hrs		**6**	**0**	**12**	**12**	**150**	**150**	**300**	
IV SEMESTER									
21LV81	Project Work II	0	0	24	12	50	50	100	EEC
Total 24 hrs		**0**	**0**	**24**	**12**	**50**	**50**	**100**	
PROFESSIONAL ELECTIVE THEORY COURSES (Four to be opted)									
VLSI System Design									
21LV21	Advanced Computer Architecture and Parallel Processing	3	0	0	3	50	50	100	PE
21LV22	Computer Aided Design for VLSI Systems	3	0	0	3	50	50	100	PE
21LV23	Electronic Packaging Technologies	3	0	0	3	50	50	100	PE
21LV24	Hardware Security	3	0	0	3	50	50	100	PE
21LV25	Low Power VLSI Design	3	0	0	3	50	50	100	PE
21LV26	Semiconductor Memory Design	3	0	0	3	50	50	100	PE
21LV27	System on Chip Design	3	0	0	3	50	50	100	PE
21LV28	VLSI for IOT Systems	3	0	0	3	50	50	100	PE

21LV29	VLSI Signal Processing	3	0	0	3	50	50	100	PE
Analog / RF Circuit Design									
21LV38	Current-mode Analog Signal Processing	3	0	0	3	50	50	100	PE
21LV30	High Speed Digital Design	3	0	0	3	50	50	100	PE
21LV31	Mixed Signal VLSI Design	3	0	0	3	50	50	100	PE
21LV32	RF Circuit Design	3	0	0	3	50	50	100	PE
21LV33	VLSI for Wireless Communication	3	0	0	3	50	50	100	PE
Nanoelectronics / Quantum Computing									
21LV34	Modelling and Simulation of Nanoscale Transistors	3	0	0	3	50	50	100	PE
21LV35	Nanoscale Devices	3	0	0	3	50	50	100	PE
21LV39	Quantum Circuit Design	3	0	0	3	50	50	100	PE
21LV36	Quantum Dot Cellular Automata Nanotechnology	3	0	0	3	50	50	100	PE
21LV37	VLSI Technology	3	0	0	3	50	50	100	PE
Open Electives									
21LV91	Smart Cities	3	0	0	3	50	50	100	OE
21LV92	Radiation Hazards	3	0	0	3	50	50	100	OE

***** Indicated is the minimum number of credits to be earned by a student.
CAT – Category; PC – Professional Core; PE - Professional Elective; RMC - Research Methodology and IPR; EEC – Employability Enhancement Course; MC - Mandatory Course; Grade – Completed / Not completed; OE – Open elective