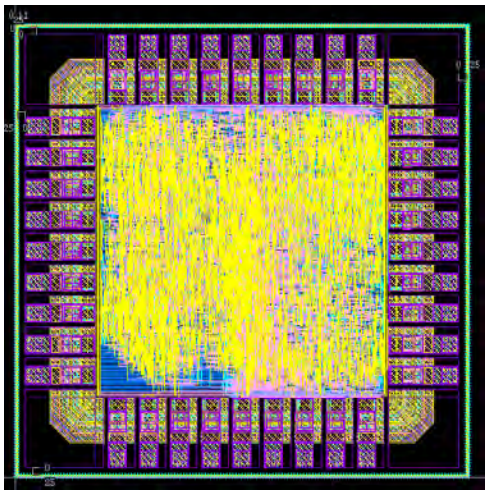
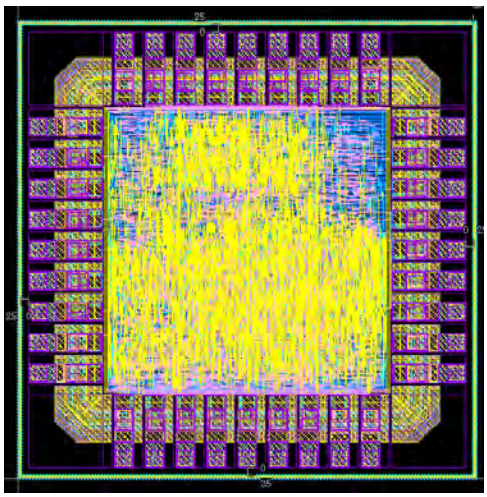
Chip Tape-out



Configurable CLEFIA Physical Layout



Configurable AES Physical Layout

The Department of Electronics and Communication Engineering, PSG College of Technology successfully fabricated two cryptographic hardware accelerators in collaboration with India's Indigenous Foundry, Semi-Conductor Laboratory (SCL), Chandigarh, Department of Space, Government of India using SCL 180 nm technology node in September 2021. The taped-out chips can be used in any security critical applications.

Members Involved

Faculty

Dr. P. Saravanan, Associate Professor, Department of ECE, PSG CT.

Research Scholar

Mrs. S. Shanthi Rekha, Full-time PhD Scholar (Visvesvaraya PhD Scheme), Department of ECE, PSG CT.

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3. Mr. G. Lakshmanan (16L119), Software Engineer, CISCO, Bangalore.
4. Ms. S. Mahalakshmi (16L120), Associate Engineer, Qualcomm, Hyderabad.
5. Mr. S. Prashanth (16L129), ASIC Engineer 1, Juniper, Bangalore.
6. Mr. S. Rajesh Srivatsav (16L132), Engineer, Arm, Bangalore.