

Chip Tape-out

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING
PSG COLLEGE OF TECHNOLOGY
COIMBATORE - 641 004

VLSI DESIGN

Successfully fabricated the following

CRYPTOGRAPHIC HARDWARE ACCELERATORS

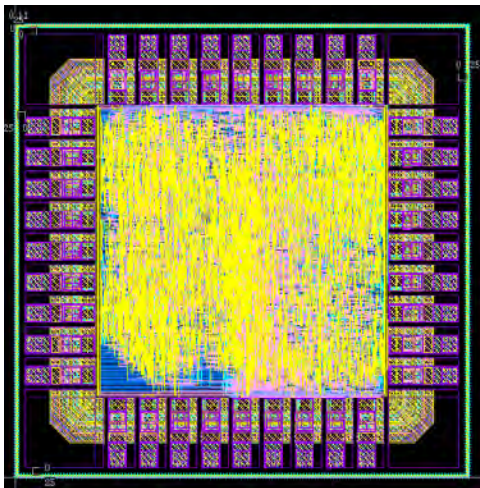
in collaboration with Semi-Conductor Laboratory (SCL), Chandigarh
September 2021



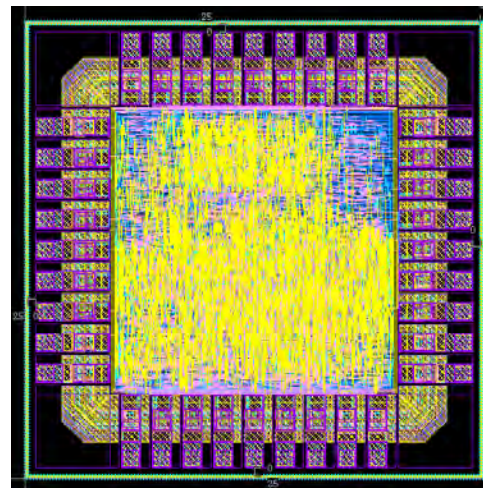
The image shows two physical chips. The left chip is labeled 'EDU11-0' and the right chip is labeled 'EDU112-0'. Both chips are marked with 'SCL-PSG', '2134802', and 'SCL INDIA'.

CONFIGURABLE CLEFIA
[ISO/IEC 29192-2:2019 Standard]

CONFIGURABLE AES
[NIST FIPS 197 Standard]



Configurable CLEFIA Physical Layout



Configurable AES Physical Layout

The Department of Electronics and Communication Engineering, PSG College of Technology successfully fabricated two cryptographic hardware accelerators in collaboration with India's Indigenous Foundry, Semi-Conductor Laboratory (SCL), Chandigarh, Department of Space, Government of India using SCL 180 nm technology node in September 2021. The taped-out chips can be used in any security critical applications.

Members Involved

Faculty

Dr. P. Saravanan, Associate Professor, Department of ECE, PSG CT.

Research Scholar

Mrs. S. Shanthi Rekha, Full-time PhD Scholar (Visvesvaraya PhD Scheme), Department of ECE, PSG CT.

Students (BE ECE 2016-2020 Batch)

1. Mr. M. Aravindh (16L106), Jr. Engineer, McKinsey, Chennai.
2. Mr. R. K. Kirubhas Shankar (16L116), Analyst, Caterpillar, Chennai.
3. Mr. G. Lakshmanan (16L119), Software Engineer, CISCO, Bangalore.
4. Ms. S. Mahalakshmi (16L120), Associate Engineer, Qualcomm, Hyderabad.
5. Mr. S. Prashanth (16L129), ASIC Engineer 1, Juniper, Bangalore.
6. Mr. S. Rajesh Srivatsav (16L132), Engineer, Arm, Bangalore.